tolerant comparator [17], improved single stage kickback rejected comparator [18], parallel prefix tree comparator [21], binary comparator [22] [28], reversible quantum comparator [29], charge sharing dynamic latch comparator [35], and switched current comparator [36]. In general, dynamic comparators could be used for high speed operations for Flash and Pipelined ADCs that used clock for the comparison process. However, dynamic comparators have large switching power dissipation as compared to pre-amplifier based comparators which are used in flash ADCs, null detectors, window detectors, zero-crossing detectors, relaxation oscillator, level shifter, site and remote sensing systems, microcontrollers, digital imaging systems, etc.

This paper presents conventional dynamic comparator in section I, section II contains dual tail comparator and section III discusses the proposed comparator. The simulated results of comparators at 180nm and 90nm technology nodes are comprised in this paper with their performance parameters such as voltage supply, propagation delay, power dissipation, and energy consumption in section IV. The conclusions and future scope of comparator designs are discussed in section V of this paper.

2 Conventional Dynamic Comparator

Conventional dynamic comparator has rail-to-rail output swing with high input impedance, and less static power consumption. The schematic diagram of the comparator is shown in Fig 1. In conventional dynamic comparator, during reset phase when clock is zero and all transistors off, a valid logical level is achieved during reset as reset transistors pull both output nodes (Out_n & Out_p) to supply voltage. During comparison phase, when clock is equal to supply voltage, tail transistor is on. Depending on the corresponding input voltage, output voltages which were pre-charged to supply voltage starts to discharge with different discharging rates.

Let $V_{IN+} > V_{IN-}$, so Out_p gets discharged faster than Out_n i.e. Out_p to fall down to $V_{DD}-|Vthp|$ before Out_n, the latch regeneration gets initiated by back-to-back inverters when corresponding PMOS transistor will turn on. Thus, Out_n gets charged to V_{DD} while Out_p drops to ground. The circuits works vice versa when $V_{IN+} < V_{IN-}$.

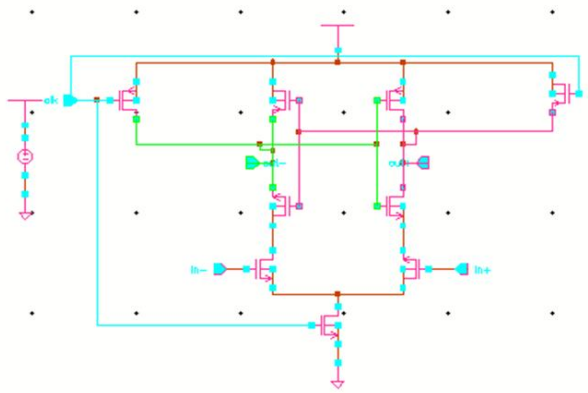

Fig1. Schematic of Conventional Dynamic Comparator

3 Double Tail Dynamic Comparator

Double Tail Dynamic Comparator has less stacking of transistors and thus it can be operated at lower supply voltages as compared to the conventional dynamic comparator. For fast latching independent of the input common-mode voltage (V_{cm}), double tail enables a large current in the latching stage with wider tail transistor, and double tail also provides a small current in the input stage for lower offset. During reset phase of comparator when clock is zero, the tail transistors are off. The intermediate nodes are charged to supply voltage. During decision-making phase when clock is equal to supply voltage, the tail transistors are on, so voltages at intermediate nodes start to drop with the rate defined by tail current and the capacitance of input transistor. The intermediate stage passes the voltage difference to the cross-coupled inverters. This stage also provides reduced kickback noise i.e. good shielding between input and output. The schematic of double tail dynamic comparator is shown in Fig 2.

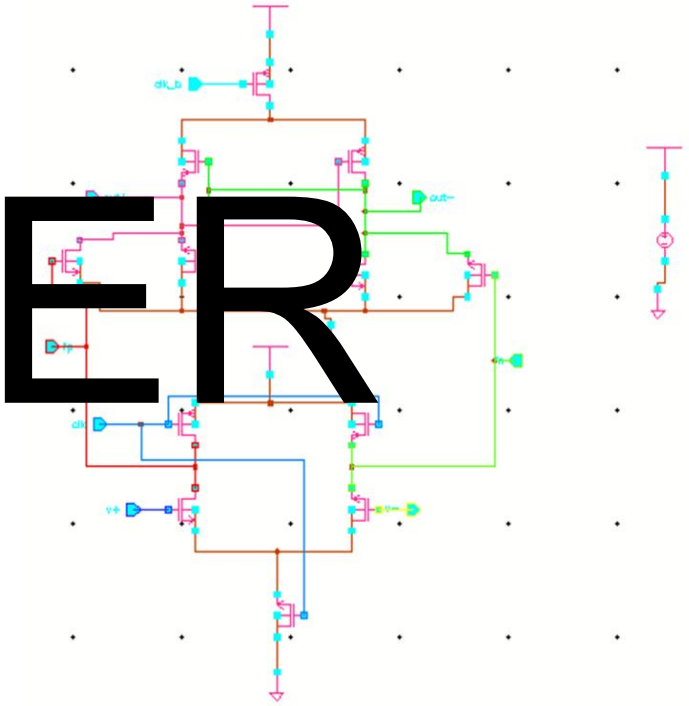

Fig2 Schematic of Double Tail Dynamic Comparator

4 Proposed Comparator

The proposed comparator is designed which is based on the double-tail topology as its performance is better in low supply voltage applications. The intermediate voltages are increased so that the latch regeneration speed gets increased by adding two control transistors to the first stage of proposed comparator in parallel to input transistors but in a cross-coupled manner as shown in schematic. During reset phase of comparator, clock is zero and the tail transistors are off, thus avoiding static power consumption, the intermediate nodes are charged to the supply voltage. During decision-making phase when clock is equal to supply voltage then the tail transistors are on. Furthermore, the control transistors are in off stage at the begin-

ning of this phase. Thus, the intermediate node voltages begin to drop in accordance of input supply with different rates.
Let $V_{IN+} > V_{IN-}$, thus positive intermediate node voltage drops faster than other one, since positive node discharge faster than the negative node. The corresponding PMOS control transistor starts to turn on as long as negative node continues falling that pulls positive node back to the magnitude of voltage supply, thus other control transistor remains off during this period that allows negative intermediate node to be discharged completely. The proposed comparator is shown in Fig 3.

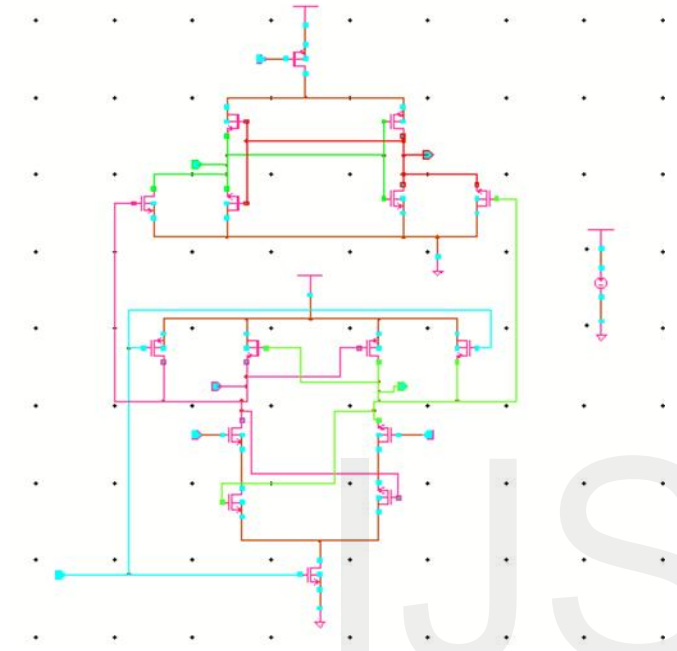

Fig3. Schematic of Double Tail Dynamic Latch Comparator

5 Simulation and Results

The Comparators are analyzed in Cadence Virtuoso Environment with a supply voltage of 600mV. Conventional dynamic comparator schematic is shown in Fig 1. The circuit is simulated with its input voltage as 300mV and reference voltage as 295mV. The clock of the dynamic comparator has amplitude of 600mV with rise and fall time of 0.08ns for a period of 1ns. The circuit is examined under transient analysis for duration of 6ns output waveforms is shown in Fig 4. The average power of conventional dynamic comparator is 12.69µW, propagation delay of 1.93ns with settling time as 5.964 ns and the speed of operation of comparator is 518.13 MHz.

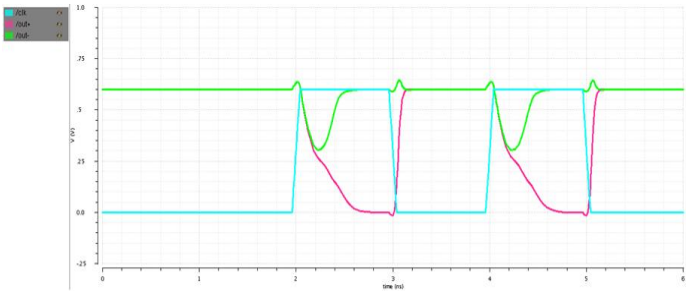

Fig4. Simulations of Conventional Dynamic Comparator

The Double Tail Dynamic Comparator is analyzed in Cadence Virtuoso Environment with a supply voltage of 600mV whose schematic is shown in Fig 2. The circuit is simulated with its input voltage as 300mV and reference voltage as 295mV. The clock of the dynamic comparator has amplitude of 600mV with rise and fall time of 0.08ns for a period of 1ns. The circuit is examined under transient analysis for duration of 6ns output waveforms is shown in Fig 5. Average Power of double tail dynamic comparator is 7.85µW, with propagation delay of 361.2ps, whereas PDP of comparator is 2.835fJ with a settling time of 5.988 ns, and energy of 0.0471pJ.

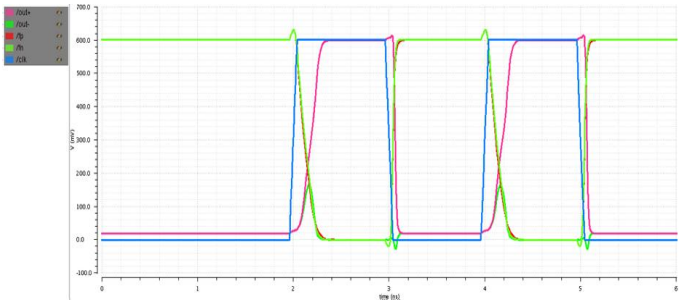

Fig5 Simulations of Double Tail Dynamic Comparator

The Proposed Comparator was designed in Cadence Virtuoso Environment with a supply voltage of 600mV whose schematic is shown in Fig 3. The circuit is simulated with its input voltage as 300mV and reference voltage as 295mV. The clock of the proposed comparator has amplitude of 600mV with rise and fall time of 0.08ns for a period of 1ns. The circuit is examined under transient analysis for duration of 6ns output waveforms is shown in Fig 6. The average power of the proposed comparator is 2.921µW with a delay of 259.7 ps so the PDP comes out to be equal to 0.7585fJ. The settling time of the waveform is 5.978 ns. The speed of operation of the comparator is 3.850 GHz.

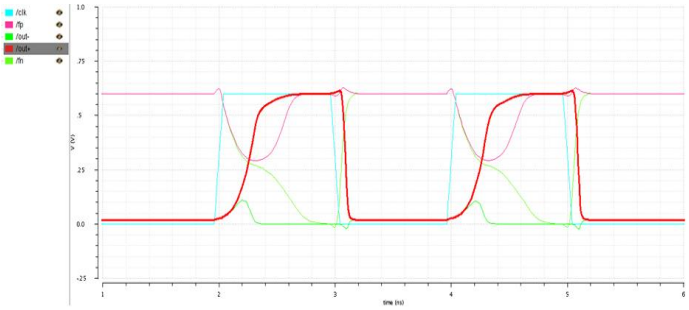

Fig6 Simulations of Proposed Comparator

The Power waveform of Proposed Comparator is shown in Fig 7 during a charging and pre-charging phase for a period of 6ns.

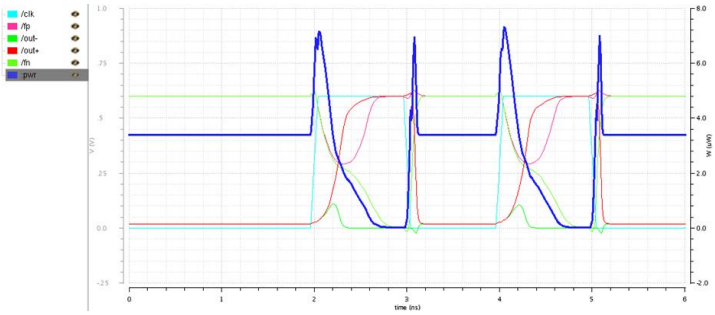

Fig7 Power Dissipation for duration of 6ns

The power consumption of conventional dynamic comparator, double tail comparator and proposed comparator is shown in Fig 8 at 180nm and 90nm technologies.

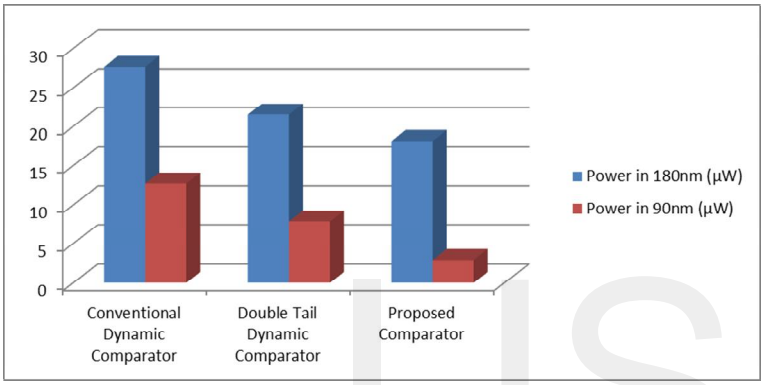

Fig8 Power of Comparator Topologies at 180nm and 90nm

The propagation delay and PDP of conventional dynamic comparator, double tail dynamic comparator and proposed comparator at 180nm and 90nm technologies is shown in Fig 9 and Fig 10, respectively.

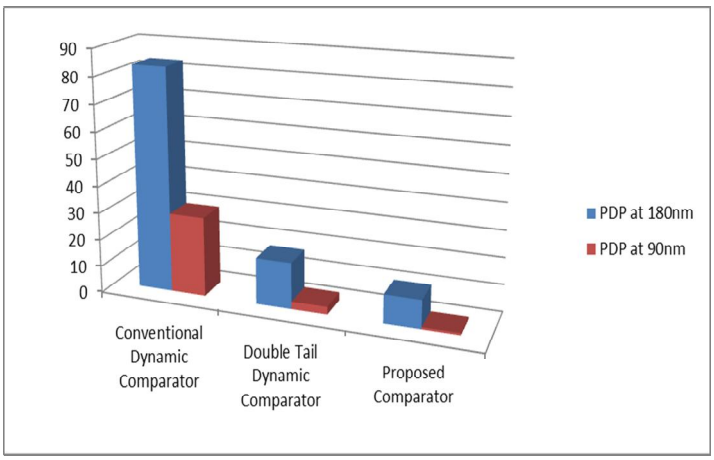

Fig9 Delay of Comparator Topologies at 180nm and 90nm Technology

The layout of conventional dynamic comparator is shown in Fig 11 which is 6.02µm* 8.105µm and layout of double tail dynamic comparator is shown in Fig 12 i.e. 8.28µm * 9.13µm in dimensions whereas the area occupied by proposed comparator is 12.82µm* 18.715µm which is shown in Fig 13 when designed in 90nm technology.

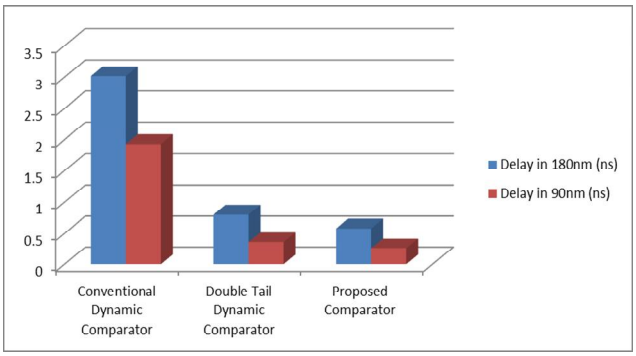

Fig10 Delay of Comparator Topologies at 180nm and 90nm

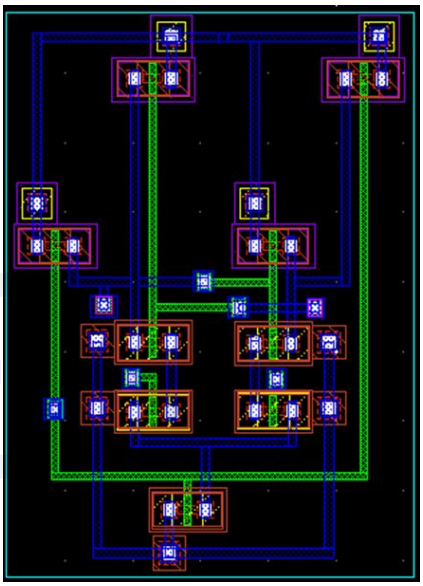

Fig11 Layout of Conventional Dynamic Comparator

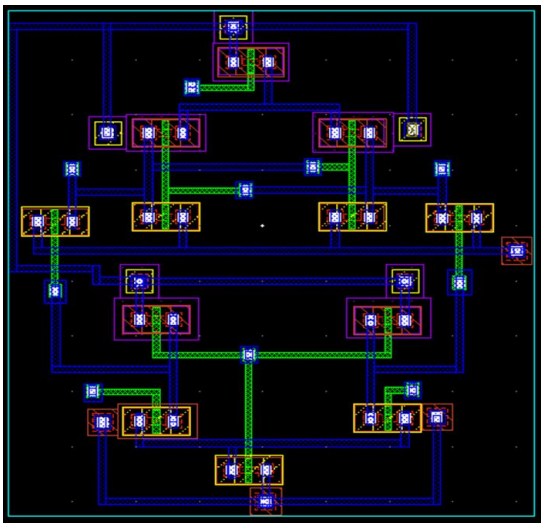

Fig12 Layout of Double Tail Dynamic Comparator

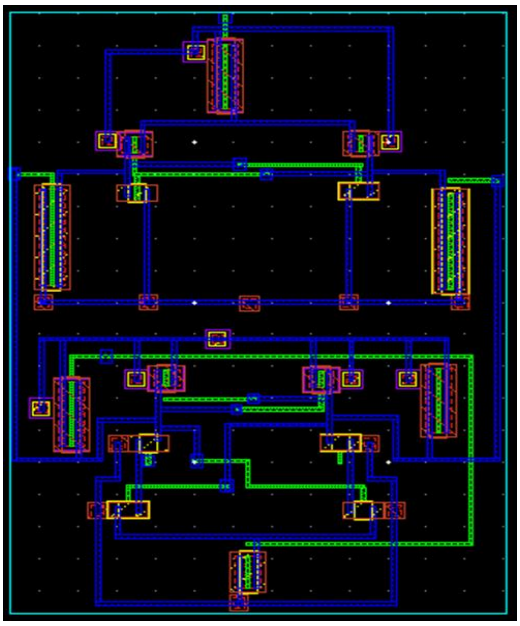

Fig13 Layout of Proposed Comparator

6 Conclusion

The results were simulated in Cadence Virtuoso Analog Design Environment with GPDK 90nm technology and 180nm technology. The proposed structure shows significantly lower power dissipation, higher speed compared to the dynamic comparators present in the literature. The average power of proposed comparator in 90nm technology is 83.92% reduced than at 180nm technology due to the decrease in channel length of the transistors and it is 62.78% reduced as compared to the double dynamic tail comparator. The delay of proposed comparator is 28% reduced when compared to the double dynamic tail comparator in 90nm technology. Thus, the proposed transistor is energy efficient when compared to other topologies at 90nm and 180nm technologies. The transistor count in the proposed comparator is more to some extent among all the comparators analyzed. From simulation results, we can see that power dissipation is more due to the switching of the transistors because of the high speed operation of the comparator, so the decreasing of dynamic power could be a work for future. The die area could be further reduced. Offset voltage optimization can be another topic of interest.

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6 Conclusion About the Authors

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Table 5.1 Comparative Analysis of Results

S. No.	Conventional Dynamic Comparator		Double Tail Dynamic Comparator		Proposed Comparator	
Technology	180nm	90nm	180nm	90nm	180nm	90nm
Average Power	27.65 µW	12.69 µW	21.53 µW	7.85 µW	18.17 µW	2.921 µW
Static Power	948nW	758nW	879nW	496nW	578nW	114nW
Dynamic Power	26.66 µW	11.932 µW	20.651 µW	7.35 µW	17.592 µW	2.807 µW
Delay	3.017ns	1.93ns	796.75ps	361.2ps	578.12ps	259.7ps
Energy	0.276pJ	0.07614pJ	0.215pJ	0.0471pJ	0.181pJ	0.01752pJ
Settling Time	9.79 ns	5.96ns	9.67 ns	5.988 ns	9.99 ns	5.978 ns
Speed	331.4 MHz	518.13 MHz	1.256 GHz	2.76 GHz	1.73 GHz	3.850 GHz
PDP	83.420fJ	24.49fJ	17.152fJ	2.835fJ	10.504fJ	0.7585fJ
Area	18.46µm * 20.03µm	6.02µm * 8.105 µm	26.945µm *36.545µm	8.28µm * 9.13µm	25.62µm* 40.11µm	12.82µm* 18.715µm