Design and Performance Analysis of Reversible Carry Look-ahead Adder and Carry Select Adder

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Abstract: Today reversible computing is more interesting research area to dwindle power consumption and reduction in heat dissipation. Reversible computing involves number of input and output lines which must be the same. Reversible computing is used in Nano-technology, low power CMOS design, Optical computing and Quantum computing .This paper shows that reversible proposed design of carry look-ahead adder using reversible Peres gate and Feynman gate to dwindle the garbage output, gate count and quantum cost as compare to existing design. The carry select adder using reversible gates is obtained with DPG gates and Modified Fredkin gates. Results are simulated in Xilinx software by using VHDL language.

Keywords
Reversible logic gates, garbage output, quantum cost, carry look-ahead adder, carry select adder.

1. Introduction

Reversibility in computing implies that information related to the computational states ought to never be lost. In Conventional computing all logical operations performed by millions of gates thus lost the bits of information and is dissipated in the form of heat. It has been shown that for every bit of information lost in conventional computations KT*log2 joules of heat energy are generated where K is Boltzmann's constant and T is absolute temperature [1] .A reversible logic gate is mandatory to have same number of inputs and outputs lines. The unique output vector produced from each input vector. This is termed as "logically reversibility". Physical reversibility is a process that dissipates no heat in terms of wastage of energy. Complexity of the circuits becomes very less owing to fewer requirements of primitive gates. Various parameters of reversible logic gates are used to design the work. Garbage output refers to the output that is not used for further computations. Constant input is also main parameter of reversible logic gates. Constant input which is used in reversible logic function to maintain constant either 0 or 1 for making it reversible. Each reversible gate has a cost associated with it called quantum cost. Quantum cost of the circuit is calculated by knowing the number of primitive reversible gates required to realize the circuit.

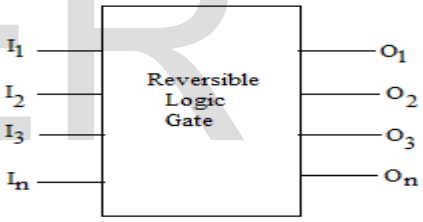

Figure1: Symbol of Reversible logic gate with n*n input and output

1.1 Organization of the work

This section describes the organization of the paper. Section 1 includes the introduction of reversibility computing. Section 2 shows the work done by the various researchers in the field of reversibility in computing. Section 3 describes the different types of the reversible logic gates. Section 4 includes the introduction of Carry Look-ahead Adder. Section 5 includes the proposed work. Section 6 includes the simulation result and compare with existing work. Section 7 includes introduction of Carry Select Adder. Section 8 includes the proposed work of Carry Select adder. Section 9 includes simulation result and compare with existing work. Section 10 includes the conclusion and future scope and then References.

2. Literature Survey

In 1961, R.LANDAUER described that the logical irreversibility is associated with physical irreversibility and

requires a minimal heat generation per machine cycle. For irreversible logic computations, each bit of information lost generates kTlog2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In conventional system the millions of gates used to perform logical operations. Author computation. The design that does not result in information loss is irreversible. A set of reversible gates are needed to design reversible circuit. Reversible gate can generate unique output vector from each input vector and vice versa [2].

In 2005 Majid Haghparast et al. proposed a novel 4*4 reversible logic gate called MKG. They designed a new reversible full-adder circuit that requires only one reversible MKG gate and produces two garbage outputs. It can be used to design efficient adders. It is shown that proposed reversible full adder is better and optimized in terms of number of reversible gates, number of garbage outputs and number of constant inputs with compared to the existing design [3].

In 2008, Majid Mohammdi et.al presented that quantum gates to implement the binary reversible logic gates. Quantum gates V and V+ to be represented in truth table forms. Author proved that several reversible circuit benchmarks are optimized and compare with existing work. A new behavioral model to represent the V and V+ quantum gates based on their properties. This model used to simulate the quantum realization of reversible circuits [4].

In 2010, D.Michael Miller and Zahra Sasanian presented the reducing the number of quantum gate cost of reversible circuits. To reduce the quantum cost improves the efficiency of the circuit. To determine a quantum circuit is to first synthesis circuits composed of binary reversible gates then map that circuit to an equivalent quantum gate realization [5].

In 2011, Prashant.R.Yelekar et.al described that reversible logic gates ability to reduce the power dissipation which is main requirement in VLSI design. Reversible computing which is requires high energy efficiency, speed and performance. It include the applications like low power CMOS, Quantum computer, Nanotechnology, Optical computing and self-repair [6].

In 2012, B.Raghu Kanth et.al described that implementing of reversible logic has advantages of reducing garbage outputs, gate count and constant inputs. Author realized Addition, Subtractions operations using reversible DKG gate and it compare with conventional gates. The proposed reversible adder/substractor circuit can be applied to design of complex systems in nanotechnology [7].

In 2012, Lafifa Jamal, Hafiz Md,Hasan Babu et.al provided the reversible carry look-ahead adder reduced the reversible gates, garbage output and quantum cost as compare to existing work. Here author also realized proposed design the reversible carry skip adder with low garbage output, quantum cost and compares it with existing work [8].

proved that heat dissipation avoidable if system made reversible [1].
In 1973, C.H.BENNETT described that if a computation carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during

In 2012, Mr. Devendra Goyal presented VHDL CODE of all Reversible Logic Gate, which are every necessary for construction of arithmetic circuits used in low power digital circuit and quantum computation. Here author have been tried to make the VHDL code as much as possible. Author can simulate and synthesis it using Xilinx software [9].

In 2013, Yedukondala Rao Veeranki1 et.al, explained the reversible TSG gate, Fredkin gate, Toffoli gate used to design the Four bit Carry bypass Adder and carry select adder. Proposed design of Carry bypass Adder and Carry Select Adder compare the power dissipation with existing work. They presented the proposed design of Carry Select adder using TSG gate and Fredkin gate. Quantum cost of reversible TSG gate is 13[12].Quantum cost of reversible Toffoli gate and Fredkin gate is 5 [10].

In 2013, Raghava Garipelly provided that the basic reversible logic gates, which in designing of more complex system having reversible circuits as a primitive component and this can execute more complicated operations using quantum computers. Author introduced some new Gates which are BSCL, SBV, NCG, and PTR etc. [11].

In 2014, Ashima Malhotra, Amandeep Singh et.al, presented the proposed reversible Multiplexers using reversible modified Fredkin gate with low quantum cost and power consumption and compare it with existing work. Proposed reversible multiplexers can be applied to design of complex systems. The results can simulate and synthesis in Xilinx by using VHDL language [12].

In 2014, Ashima Malhotra et.al, described that reversible modified Fredkin gate used to design the multiplexers with low quantum cost and compare it with existing work. They also compare the quantum cost of multiplexers design using Fredkin gate with Modified Fredkin gate used to design he multiplexers [13].

3. Different Types of Reversible Logic Gates

3.1 Feynman Gate

Feynman gate is a 2x2 reversible gate. The input vector is I(A,B) and the output vector is O(P,Q).The output defined by P=A,Q=A$\oplus$ B. Quantum cost of a Feynman gate is 1.Feynman gate can be used as copying gate.

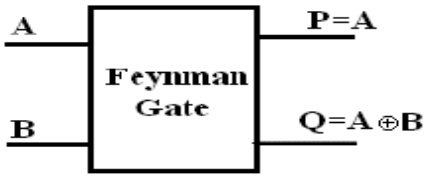

Figure2: Symbol of Feynman gate

3.2 Toffoli Gate

Toffoli gate is 3x3 reversible gate. The input vector is I(A,B,C) and the output vector is O(P,Q,R).The outputs are defined by P=A,Q=B,R=AB⊕C. Quantum cost of a TOFFOLI gate is 5.

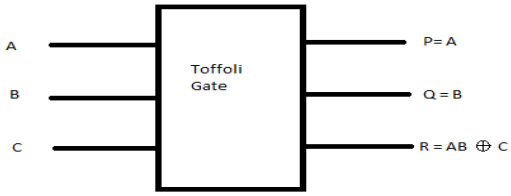

Figure3: Symbol of Toffoli gate

3.3 Peres Gate

Peres gate is 3x3 reversible gate. The input vector is I(A,B,C) and the output vector is O(P,R,S).The output is defined by P=A,Q=A⊕ B and R=AB⊕C. Quantum cost of a Peres gate is 4.

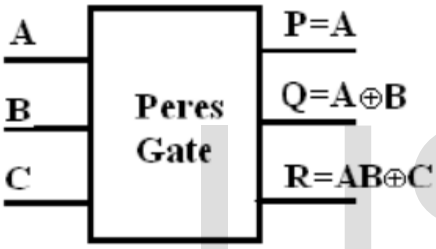

Figure4: Symbol of Peres gate

3.4 Modified Fredkin Gate

Fredkin gate is 3x3 reversible gate. The input vector is I(A,B,C) and the output vector is O(P,Q,R).The output is P=A,Q=AB'⊕ AC' and R=A'C⊕AB. Quantum cost of Fredkin gate is 4.

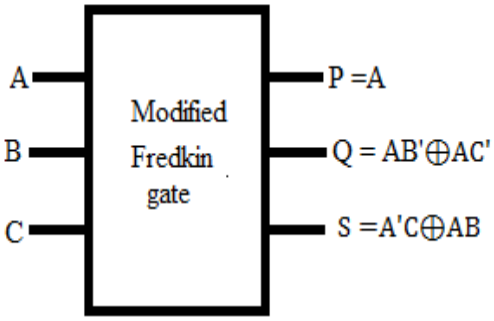

Figure5: Symbol of Modified Fredkin gate

3.5 Double Peres Gate (DPG)

DPG gate is 4x4 reversible gate. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S).The output is P=A,Q=A⊕B,R=A⊕B⊕D and S=(A⊕B)D⊕AB⊕C. Quantum cost of DPG gate is 6.It can work singly as Reversible full adder with C=0 and D=Cin.

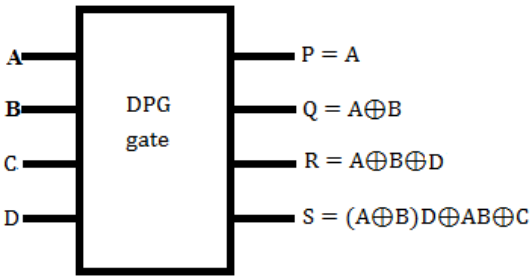

Figure6: Symbol of DPG

4. Carry Look-ahead Adder

Carry look-ahead adder are fastest adder of all adders because it calculates the carry bits before the summation. Carry look-ahead adder actually determines the carry bit by two modules first is "generate a carry" and second is "propagate a carry". Carry signal will be generated in two conditions. When both bits Ai and Bi are equal to 1 or when carry-in is 1 and Ai or Bi is 1.

Carry propagation (Pi) and Carry generation (Gi) are

Pi = Ai ⊕ Bi

Gi = Ai Bi

Sum signal can be calculated as follows:

Si = Ai ⊕ Bi ⊕ Ci = Pi ⊕ Ci

Carry signal can be calculated as

Ci+1 = Gi ⊕ Pi Ci

Applying this to a 4-bit adder ,we have:

C1 = G0 ⊕ P0C0

C2 = G1 ⊕ P1C1 = G1 ⊕ P1(G0 ⊕ P0C0)

C3 = G2 ⊕ P2C2 = G2 ⊕ P2(G1 ⊕ P1C1)

Partial Full Adder (PFA): This adder generates Gi, Pi and Si.

Pi = Ai⊕Bi, Gi= Ai.Bi, Si= Ai⊕Bi⊕Ci

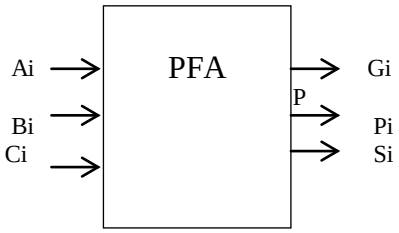

Figure7: Symbol of Partial Full Adder (PFA)

5. Proposed Work

The proposed design 4-bit carry look-ahead adder using Peres gate and Feynman gate as compare to existing works This used Peres gate, Toffoli gate and Feynman gate. The proposed method overcomes the quantum cost, gate count and garbage output as compare to existing work. Peres gate used to generate carry propagation Pi = Ai xor Bi and carry generation Gi = Ai and Bi. Architecture of proposed 4-bit reversible carry look-ahead adder shown in Figure 10. Feynman gate is used as coping gate which generate the number of Pi and Gi. Take the initial input carry C0 equal to 0.With the help of Feynman gate sufficient amount of Pi and Gi to calculate sum.

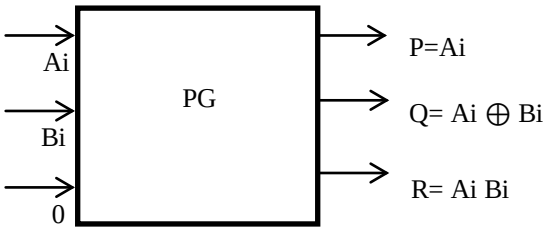

Figure8: Reversible Peres gate used as carry propagator and carry generator

Reversible Peres gate is 3x3 gate. Input vector Ai, Bi, and Ci=0 output will be P=Ai, Q= Ai xor Bi, R= Ai and Bi.
The output vector Q is used to generate carry propagation Pi and output vector R is used to generate carry generation Gi.

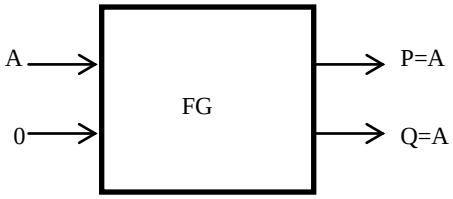

Figure9: Reversible Feynman gate used as coping gate

It uses eight Feynman gates (FG) and eight Peres gates (PG).It has four bit carry look-ahead adder calculate the s0,s1,s2,s3 and carry outputs and also has ten garbage outputs. This proposed 4-bit carry look-ahead adder has Quantum cost of 40.

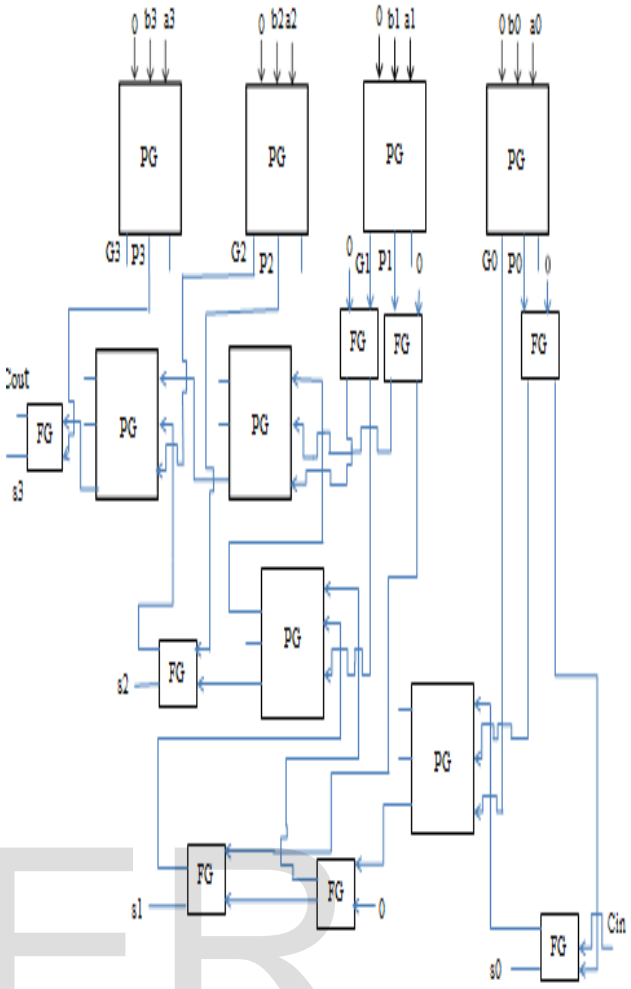

Figure10: Architecture of proposed 4-bit reversible carry look-ahead adder

6. SIMULATION RESULT

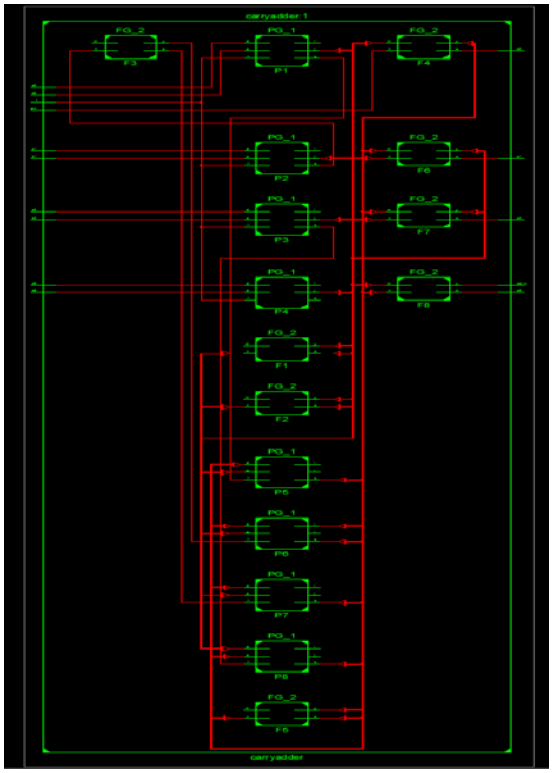

Figure11: RTL view of 4-bit Carry Look-ahead adder using Peres gates and Feynman gate

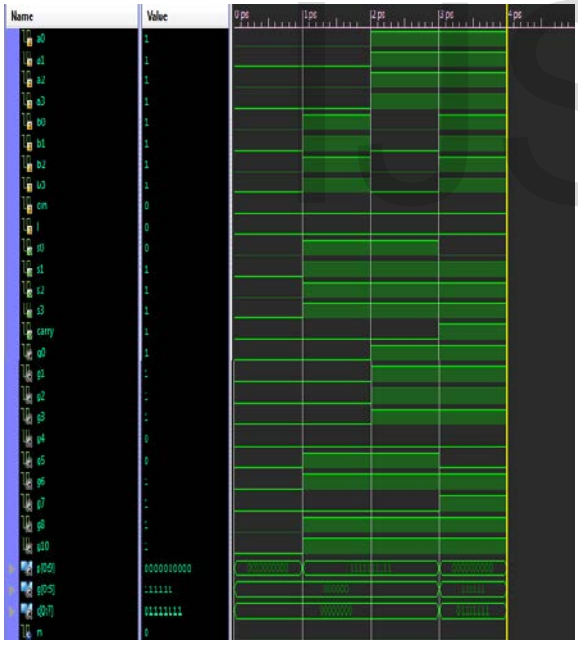

Figure12: Simulation waveform of 4-bit reversible Carry Look-ahead Adder

Table1: Comparison of Proposed work with Existing work

	Kinds of gates	Quantum Cost	Garbage output
Proposed Design	2	40	10
Existing Design[8]	3	56	14

7. Carry Select Adder

Carry Select Adders are one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. The carry-select adder partitions the adder into several groups, each of which performs two additions in parallel. Two four bit ripple-carry adders are used to generate carry per select stage. One ripple-carry adder evaluates the carry chain assuming the carry-in is zero; second ripple-carry adder assumes carry-in to be one. Once the carry signals are computed, the correct sum and carry-out signals will be simply selected by a set of multiplexers.

8. Proposed Work

Proposed design of Carry Select adder using reversible gates is obtained with eight DPG gates and five Modified Fredkin gates. The three input Modified Fredkin gate serves as multiplexer. Quantum cost of reversible Double Peres gate (DPG) is 6 and Quantum cost of Modified Fredkin gate is 4.Architecture of proposed 4-bit Carry Select adder shown in Fig.13.Two four bit ripple-carry adders using reversible eight DPG gates to generate carry per select stage. Proposed work with low Quantum cost and garbage output as compare to existing work. Carry select adder design by using reversible TSG gate and Fredkin gate in existing work. Quantum cost of TSG gate is 13 and Quantum cost of Fredkin gate is 5.

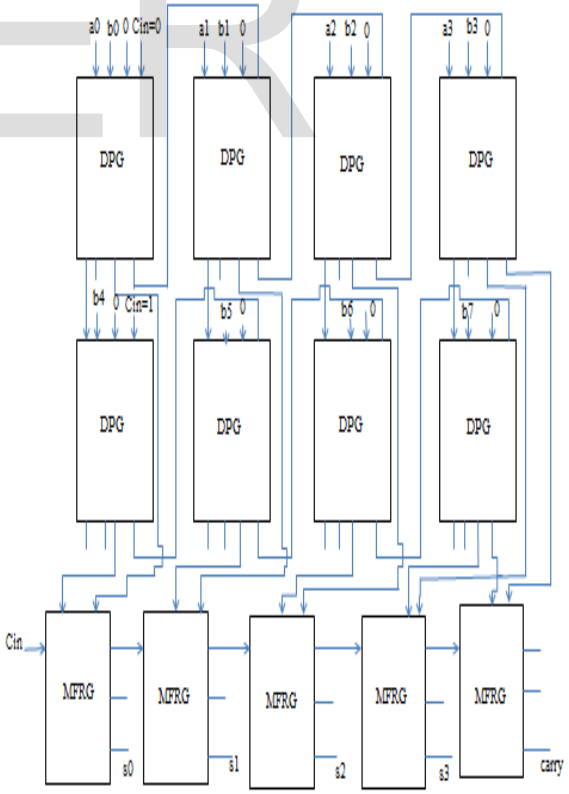

Figure13: Architecture of proposed 4-bit reversible Carry Select Adder using DPG and Modified Fredkin gates

9. Simulation Result

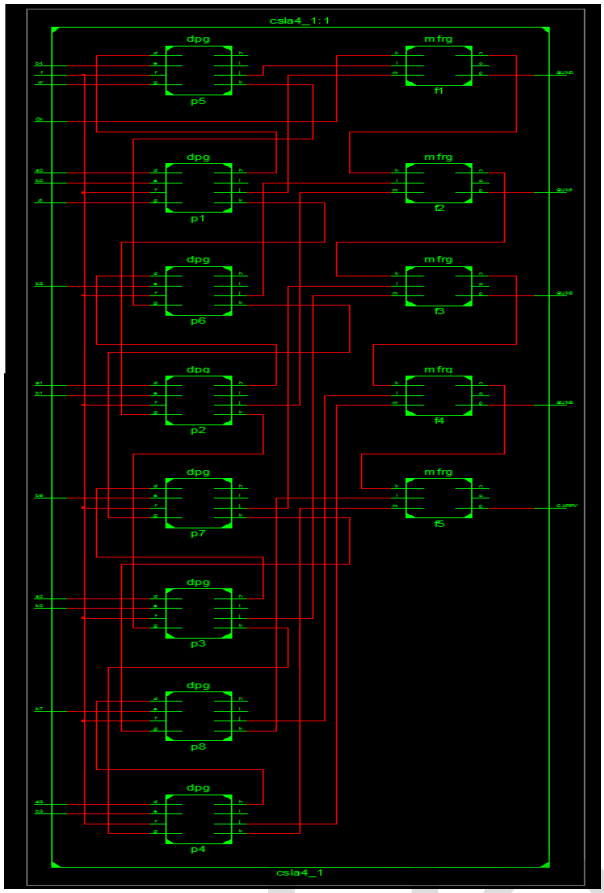

Figure14: RTL view of Carry Select Adder using reversible DPG and Modified Fredkin gate

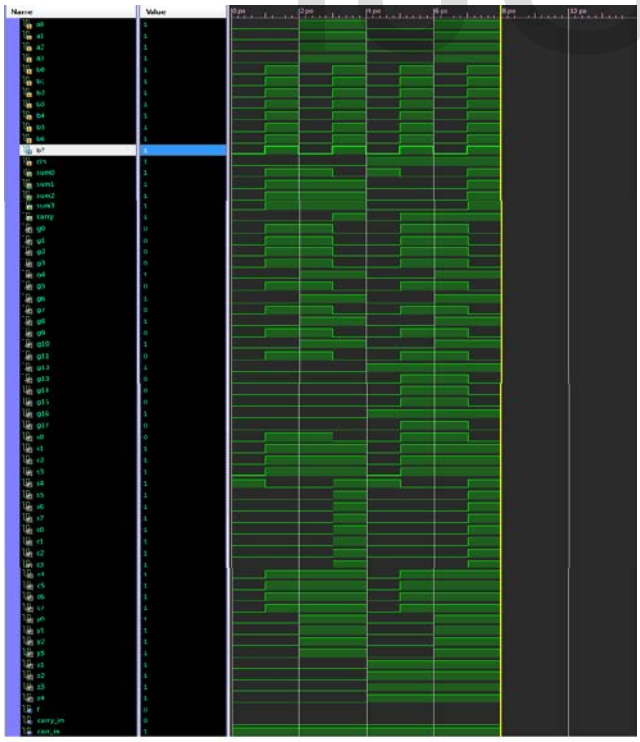

Figure15: Simulation waveform of 4-bit reversible Carry Select Adder

Table2: Comparison of Proposed work with Existing work

	Quantum Cost	No. of Garbage Output
Proposed Design	68	17
Existing Design[10]	129	25

10. Conclusion and Future Work

Reversible computing has its great significance in diminishing the complexity of the digital circuits. In this paper we are presented 4-bit Carry Look-ahead Adder using reversible Peres gates and Feynman gates with low quantum cost and low garbage outputs as compare to existing work [8]. We are also presented 4-bit Carry Select Adder using reversible DPG gates and Modified Fredkin gates with low quantum cost and low garbage outputs as compare to existing work [10].Reversible computing is becoming an important research area include Quantum computing, Nanotechnology, Low power CMOS design, Spacecraft, Cryptography, Digital signal processing.

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